Power Transistors: MOSFETs

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I. Introduction

This document discusses power MOSFETs, primarily dealing with its principle of operation, the static characteristics, and the symbol and equivalent circuit. After that, the switching characteristics are discussed, aiming to achieve the expressions that govern the commutations in HF switching power electronic converters. Ultimately, the switching and conduction losses in these semiconductors will be analyzed.

II. Principle of operation of a MOSFET

The typical structure of a Metal-Oxide-Semiconductor Field-Effect Transistor, MOSFET, is shown in figure 1.a. Three different doped regions are present, a Source (S), a Substrate and a Drain (D). The Substrate has a dopant material that is opposed to the doping of the Drain and the Source. In this case, drain and source are N region, while the Substrate is a P region. The Gate (G) is a metallic terminal that is joined to the silicon through an oxide material. Hence there is no direct connection between the gate and the rest of the transistor. In fact, the gate-to-source equivalent of the MOSFET is a capacitor, in series with an internal resistor.

There are two PN junctions, i.e. two diodes, in a typical MOSFET structure. These diodes are represented in figure 1.b. A diode from the Substrate to the Drain and a diode form the Substrate to the Source. It must be remarked that the Substrate is connected externally (by means of the metallic contact) to the Source. Therefore, the source-to-substrate diode is shorted. As a consequence, only the Drain to Source diode, must be considered. This diode will play a very important role in some power electronic applications.

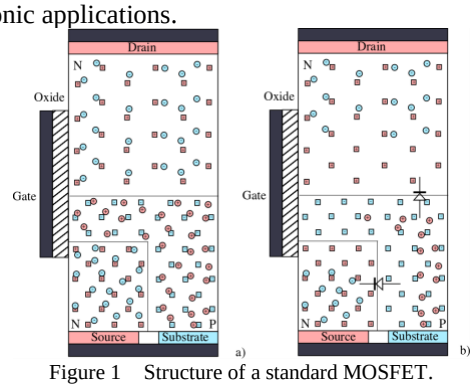

Figure 1 Structure of a standard MOSFET.

Figure 2.b also shows the 2 depletion regions that appear in the MOSFET, when the depletion field compensates the diffusion current, to reach the equilibrium (exactly as in the case of depletion regions in a standard diode or in the BJT transistor).

Cut-off region.

Usually, the DS junction is reverse biased, meaning that the u_{DC} voltage is relatively large (typically some hundreds of volts). While this DS diode is reverse biased no current flows. The limit breakdown voltage that the device is able to withstand is related with the concentration of dopant materials. The Drain is lightly doped (N-) close to the substrate in order to increase this voltage level.

In the cut-off region, no voltage, and thus no charge, is present in the gate. The device acts as a reverse biased diode.

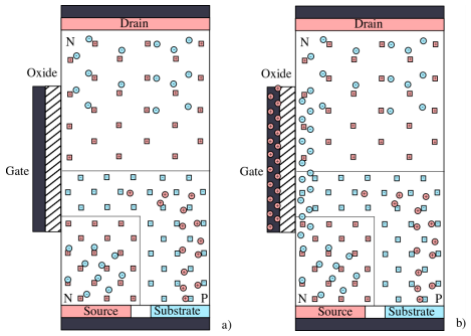

Figure 2 A N-channel MOSFET, in the off-state (a) and with a gate voltage (b). A channel of n carriers appears between drain and source.

Forward bias of the MOSFET

When a voltage appears in the gate, the gate-source dipole behaves as a capacitor. Assuming a positive voltage in the gate, an amount of positive charge appears in the gate. In this case, the same amount of negative charge flows towards the section of the transistor opposite to the gate. Therefore, a channel of e^- carriers (N-Channel) appears on the drain.

Given that a large voltage v_{DS} is applied externally, a current, I_S, flows from the drain to the source. The current flow is limited by the resistivity of the material. This resistivity ids dominated by the resistance of the N- region (lightly doped), and it's called $R_{DS(on)}$. This resistance increases for devices with higher maximum V_{DS} values, as the higher the dopant concentration, the larger the number of free carriers able to transport charge.

III. Static Characteristic of Power MOSFETs

The characteristics of the MOSFET transistor can be studied considering the voltage v_{DS} is large (reverse bias of the DS diode) and v_{GS} initially zero, but increasing gradually.

Figure 3 shows the relevant regions in the MOSFET characteristic.

Initially, if v_{GS} is zero, the channel is not present in the structure (Figure 4.a). The characteristic is thus the one corresponding to a reverse biased diode, and as the v_{DS} increases, a small reverse current flows. This is the cut-off region, used to block large drain-to-source voltage levels. This situation remains as it is until v_{DS} reaches a given breakdown value (as in the regular PN junction), where a large current starts to flow, usually destroying the device. This characteristic is plotted in Figure 3 as v_{GS0}.

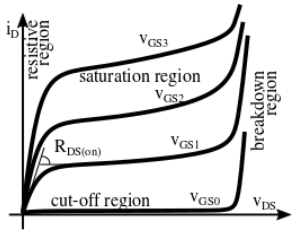

Figure 3 Structure of a standard MOSFET.

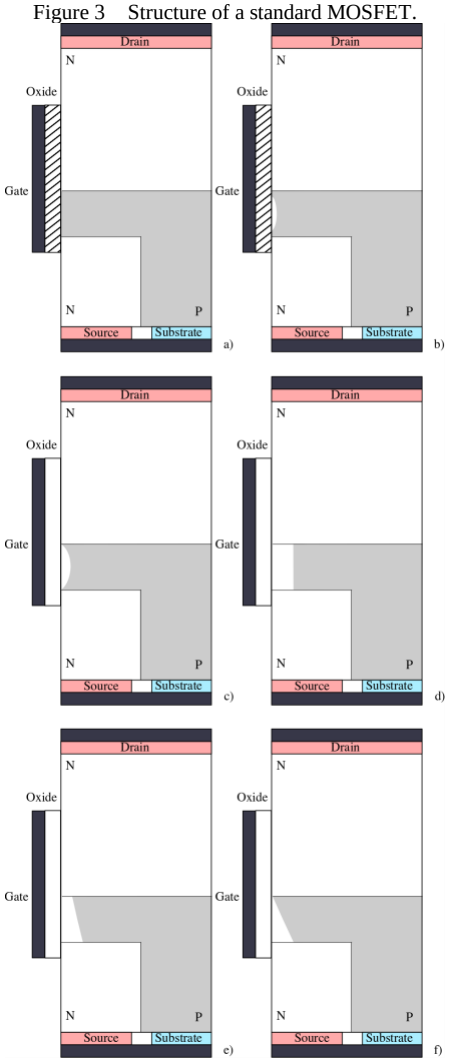

Figure 4 Charge distribution in the Substrate, close to the gate, and channel formation. a) For v_{GS} voltage equals to zero. b) For a v_{GS} value below the threshold value. c) For the exact threshold value. d) For voltage v_{GS1}, above the threshold value, with small v_{DS} value. e) For voltage v_{GS1}, above the threshold value, with greater v_{DS} value . f) For voltage v_{GS1}, above the threshold value, with greater v_{DS} value (saturation or active region).

For v_{GS} voltages greater than zero, but below a certain threshold value, the charge distribution in the gate follows the structure shown in figure 4.b, and still the channel is not properly generated. Even though there are some charges stored in the substrate, the channel is not formed, as the e^- carriers close the PN junctions tend to avoid these areas (accelerated by the depletion field). Therefore, the device still presents the cut-off behavior.

At the threshold level, i.e. $v_{GS}=v_{GS(th)}$, the distribution of the e^- carriers in the gate is as the one in Figure 4.c. For voltages greater than this threshold value (e.g. v_{GS1} in figure 3), the charge distribution in the device is similar to the one depicted at figure 4.d. At this time, an effective channel exists, with a given width given by the voltage level v_{GS1}. In this situation, if the v_{DS} voltage level starts to increase from zero, the e^- carriers will flow, accelerated by the external field. The ratio of v_{DS} voltage to i_D current is given by the resistance of the semiconductor, mainly dominated by the channel resistor. This value is called turn on resistor, $R_{DS(on)}$. For relatively small v_{DS} voltages, the value of $R_{DS(on)}$ remains more or less constant.

However, if v_{DS} increases, the channel distribution evolves as in Figure 4.e. The e^- carriers in the channel tend to move away from the depletion area close to the drain. The p^+ charges in the gate tend to move away from the drain (that has a large positive voltage). In addition, as the field in the Drain-to-Substrate depletion is large, the carriers tend also to move away from this junction. So, effectively the channel depth decreases, somehow limiting the drain current i_D.

Finally, for large v_{DS} values, the channel is pinched-off at the drain region, and as a result the channel does not cover the full gate region. The current, though, still flows due the high external field (e^- have such energy that "jumping" the region without a channel), but it is mainly independent of v_{DS}. The value of the current i_D is a function of the v_{GS} gate to source voltage.

IV. MOSFET Symbol and equivalent circuit

Figure shows the N-channel enhanced MOSET discussed in the above sections. The gate circuit can be modelled by a capacitance and an internal resistor, R_G.

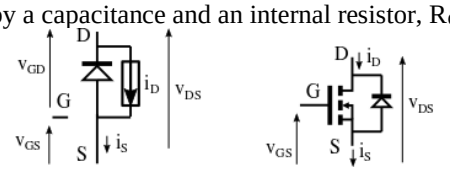

Figure 5 a) Simplified equivalent circuit of the MOSFET. b) Symbol of the N-Channel enhancement MOSFET.

V. Majority carrier device

The charge is transported only by the (-) carriers, which are majority carriers in the N regions, and also in the N channel that is formed by the voltage in the gate. Therefore, **MOSFETs are majority carrier devices.** This statement has some implications [2]:

- Unlike in minority carrier devices (as a standard PN diode), there is not conductivity modulation, and the $R_{DS(on)}$ resistance can take large values for designs of large breakdown voltages.
- An extra consequence is that these devices are generally faster than minority carrier devices (no need to remove minority charge stored close to the PN junctions).

Thermal Behavior

MOSFETs exhibit positive thermal coefficients. The larger the temperature, the larger the $R_{DS(on)}$. This is due the channel behaving like a conductor. The more temperature, more vibration in the atoms within the channel, that tends to oppose the free movement of electrons. These vibration increases the probability of electrons colliding with atoms; the carriers lose kinetic energy, and the effective charge transport is reduced [2]. The global result is that the resistance increases with temperature.

This is very important, since it enables easy parallelization of switches, as the positive thermal coefficient allows for a natural equalization of currents.

In the case of BJTs transistors and PN diodes, the thermal behavior implies a negative thermal coefficient in the ON state resistance. The larger the temperature, the more electrons reach the conduction band, and the more holes appear at the valence band. This implies more mobility of majority and minority carriers, effectively decreasing the resistance.

VI. Conduction Losses

Conduction losses on a power MOSFET are modelled with a turn-on equivalent, equal to a pure resistor, $R_{DS(on)}$, that changes with the operating conditions.

For standard MOSFET, the maximum temperature can be considered to be 120ºC, whereas for SiC MOSFET, it can be assumed even higher than 150ºC.

In any case, a close look to the datasheet of the device (in figure 6 a standard Si MOSFET is depicted), can show how the $R_{DS(on)}$ at 25ºC (0.33Ω) must be multiplied by a factor of 2 for 120ºC, yielding up to 0.67Ω. If this plot is not present, then a simple interpolation with 25ºC and 150ºC must be carried out, by using figure 7.

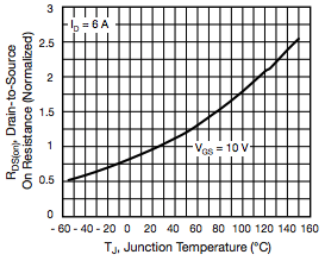

Figure 6 Normalized On-Resistance vs. temperature

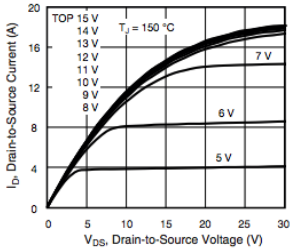

Figure 7 Typical Output characteristics

The expression then of the conduction losses is, thus:

$$P_{LOSS,S,Cond} = \int_{t=0}^{t=D\cdot T} (i_L(t)^2 \cdot R_{DSON}) \cdot dt \qquad (1)$$

Table I: Parameters for Conduction Losses

Parameter	Units	Description
D	p.u.	Duty ratio
f_{SW}	Hz	Switching frequency
$i_L(t)$	A	Current through the inductor as a function of time (equal to the MOSFET $i_S(t)$ current when the switch is turned on).
$R_{DS}(on)$	Ω	Turn-on DS resistor

VII. Switching Losses

The parameters that affect the switching transients are the voltage and current steady state vales, the driver characteristics (voltage values and resistances), the internal capacitances and resistors of the switch, inductances due the circuit layout, as well as parameters of the rectifier diode. These parameters, depicted in Figure 8 in the case of a resistive load (represented by RL) are summarized in table II.

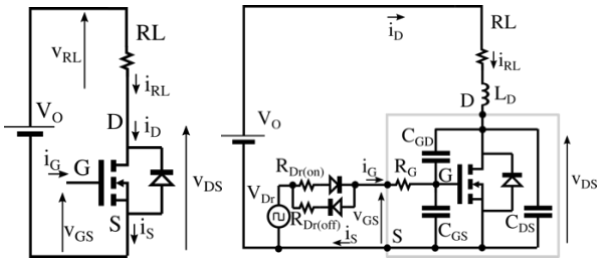

Figure 8 Equivalent circuit of the MOSFET and driver for resistive switching. Left: references at the main devices. Right: Detailed model of the switch and driver.

Table II: Parameters for Switching Losses

Parameter	Units	Description
V_O	V	Switching Voltage
I_L	A	Switching Current
$V_{Dr(on)}$	V	Turn-on voltage of the driver
$V_{Dr(off)}$	V	Turn-off voltage of the driver
$R_{Dr(on)}$	Ω	Driver turn-on resistor (ext.)
$R_{Dr(off)}$	Ω	Driver turn-off resistor (ext.)
R_G	Ω	MOSFET internal gate resistor
C_{GD}, C_{GD0}	F	MOSFET internal GD Capacitor.
C_{GS}	F	MOSFET internal GS Capacitor
C_{DS}	F	MOSFET internal DS Capacitor.
g	Ω^{-1}	MOSFET transconductance
Q_{GD}	C	MOSFET Gate to Drain charge
$V_{GS(th)}$	V	Threshold value (take typ value)
L_D	H	Parasitic inductance of drain path
I_{rr}	A	Reverse recovery peak current of diode R
$I_{OH(PEAK)}$	A	"High" peak output current of driver
$I_{OL(PEAK)}$	A	"Low" peak output current of driver
$V_{OH(MAX)}$-$V_{Dr(on)}$	V	High Level output voltage (to V_{CC} Driver)
$V_{OL(MAX)}$	V	Low Level output voltage

a) Transconductance, g.

The transconductance is given by:

$$g = \frac{i_D}{v_{GS} - v_{GS(th)}} \qquad (2)$$

However, this is one of the most varying parameters in the MOSFET, and therefore its value must be selected carefully. An accurate estimation of this parameter is not easy. The value of the transconductance, g, largely depends on the operation conditions. For instance, for small drain currents and gate-to-source voltage values (e.g. at turn-on), the value of the transconductance is significantly smaller than at rated values (e.g. at turn on). The datasheets provide a value for the transconductance that is usually at steady state, and does not consider variations that might affect the switching transients.

This is also related with the variation of the threshold voltage that might be considered, existing a very large variation of values depending on the conditions.

b) Parasitic Capacitances, C_{iss}, C_{oss}, C_{rss}.

The internal equivalent circuit of the MOSFET at Figure 8 is assumed [1]. Here, the parasitic capacitances, C_{GD}, C_{GS} and G_{DS} are shown. The capacitances provided by the manufacturer usually are the effective input, output and reverse transfer capacitances, C_{iss}, C_{oss}, and C_{rss}, respectively. The following relationships can be derived:

$$C_{iss} = C_{GD} + C_{GS} = C_G \quad (3)$$

$$C_{oss} = C_{DS} + C_{GD} \quad (4)$$

$$C_{rss} = C_{GD} \quad (5)$$

And therefore:

$$C_{GD} = C_{rss} \quad (6)$$

$$C_{GS} = C_{iss} - C_{rss} \quad (7)$$

$$C_{DS} = C_{oss} - C_{rss} \quad (8)$$

It must be noticed that the manufacturer usually gives 2 values for this capacitance, one for active region, C_{GD} (valid for $v_{GS} << v_{DS}$), and the other for ohmic region, C_{GDo} (valid for $v_{GS} \geq v_{DS}$, typically $v_{DS}=I_L \cdot R_{DSON}$).

It must benopticed that, generally speaking, these capacitances, specially C_{GD}, changes very significantly with the DS voltage (Figure 9).

This yields inaccurate expressions if the usual capacitance equations are used.

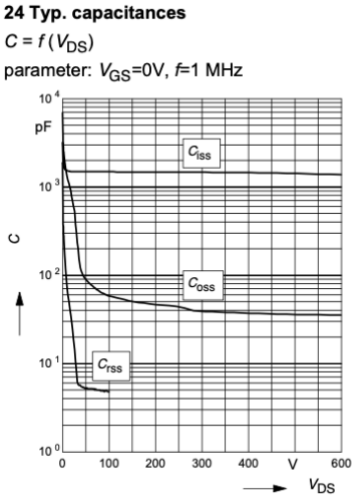

Figure 9 Variation of capacitances with drain to source voltage.

c) Parasitic inductances, L_G , L_S and L_D

Also, a leakage inductor at any of the terminals of the switch can be considered. For instance, Figure 8 shows this element at the Drain, L_D. This device is hard to quantify, but it can be assumed to be 1nH/mm of PCB track [3].

Particularly, the inductor in the gate-to-source loop, L_{GS} is critical to avoid spurious turn-on or turn-off of the switch. This practically limits the values of the gate resistors. It can be neglected if Kelvin connection is used.

d) External gate resistors, $R_{Dr(on)}$, $R_{Dr(off)}$

Moreover, an internal gate resistor, R_G, is considered. The overall resistance to turn on and off is a combination of the internal resistor, R_G, and the external resistor at the driver, $R_{Dr(on)}$ and $R_{Dr(off)}$, respectively, so that:

$$R_{ON} = R_{Dr(on)} + R_G \quad (9)$$

$$R_{OFF} = R_{Dr(off} + R_G \quad (10)$$

These values are limited by several reasons. For instance, the maximum gate current through the driver must be ensured, and therefore:

$$R_{Dr(on)} \geq \frac{V_{Dr(on)} - V_{Dr(off)} - V_{OL(MAX)}}{I_{OL(PEAK)}} - R_G \quad (11)$$

$$R_{Dr(off)} \geq \frac{V_{Dr(on)} - V_{Dr(off)} + V_{OH(MAX)} - V_{Dr(on)}}{I_{OH(PEAK)}} - R_G \quad (12)$$

Also the power dissipation in the driver must be kept below limits.

And also, spurious turn on and off due the parasitic elements must be avoided. In order to avoid parasitic turn on this, the following equation must be fulfilled:

$$R_{Dr(off)} \leq \frac{V_{GS(th)} - V_{Dr(off)}}{C_{GS} \cdot \frac{dV}{dt}} - R_G \quad (13)$$

VIII. Inductive Switching Characteristics and Power Losses

By far the most common switching scheme in power MOSFETS is the inductive switching that can be simplified by the circuit sketched in Figure 10.

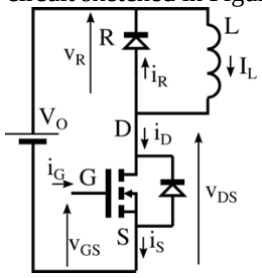

Figure 10 Inductive switching scheme.

For such switching case, the assumption is that during the switching transients, the load current is constant. This is the case of an inductive load (L). In order to study the switching characteristics of a power MOSFET, an inductive switching transient will be studied, considering the internal equivalent models of the transistor and driver shown in Figure 11.

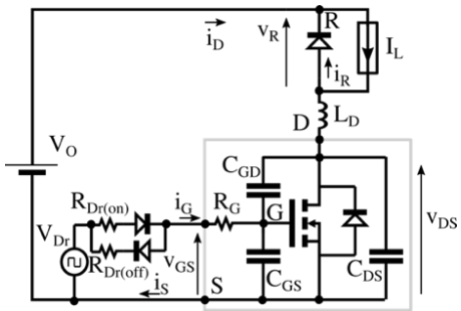

Figure 11 Equivalent circuit of the MOSFET and driver for inductive switching.

IX. Turn-on Power Losses in Inductive Switching

Initially, the switching transients at turn-off for the MOSFET will be studied, considering no reverse recovery phenomenon in the associated diode (R). This is true in the case of assuming an ideal rectifying diode, but also in the case of considering SiC Schottky power diodes. In any case, and for illustration purposes, the complete situation considering the reverse recovery peak will be only introduced after studying the initial case, modifying the initial formulas. However, the final formulas for the complete case degenerate to the ideal diode ones by

making one parameter equals to zero (I_{rr}=0). Therefore, the complete formulas can be always considered.

a) Turn-on Switching Transient with Ideal Rectifying Diode (without Reverse Recovery Phenomenon).

The diode R is considered ideal in a first approach. In this case, the turn on transient is given by the waveforms in Figure 12.

Initially, the transistor is turned off. The gate to source voltage is low (negative), the drain to source voltage is large, and the drain current is zero. Because of the inducive load, a current is flowing through the inductor L and the diode R.

- Interval t_0-t_1

The driver voltage turns on at t_0. Initially, capacitance C_G (actually formed by the parallel of C_{GS} and C_{GD}) is charged through the resistor R_{ON}, following an exponential function:

$$v_{GS}(t) = \left(V_{DR(on)} - V_{DR(off)}\right) \cdot \left(1 - e^{-\frac{t-t_0}{R_{ON}\cdot\left(C_{GD(hv)}+C_{GS}\right)}}\right) \quad (14)$$

It must be noticed that the value of CGD considered is the one corresponding to high voltage in the drain to source, $C_{GD(hv)}$.

Nothing happens at the Drain, until the GS voltage reaches the threshold value, $V_{GS(th)}$, in t_1. The interval t_1-t_0 can be obtained by solving the exponential equation that defines this charging.

$$t_1 - t_0 = -R_{ON} \cdot \left(C_{GD(hv)} + C_{GS}\right) \cdot ln\left(1 - \frac{V_{GS(th)}-V_{DR(off)}}{V_{DR(on)}-V_{DR(off)}}\right) \quad (15)$$

- Interval t_1-t_2

From t_1 onwards, the exponential charging at the gate continues, but now the drain current starts to increase from 0 to the inductance current value, I_L. Given that the inductor current remains constant during the switching interval, the diode current decreases correspondingly from the I_L value to 0 (in grey in figure 10).

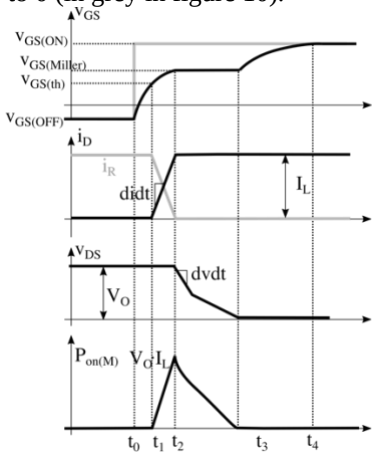

Figure 12 Waveforms at turn on (ideal rectifier diode).

But the drain voltage does not change, and the drain current is a function of the transconductance, g, and the GS voltage. Therefore:

$$v_{GS}(t) = \left(V_{DR(on)} - V_{DR(off)}\right) \cdot \left(1 - e^{-\frac{t-t_0}{R_{ON}\cdot\left(C_{GD(hv)}+C_{GS}\right)}}\right) \quad (16)$$

$$i_D(t) = \mathrm{g} \cdot \left(v_{GS}(t) - v_{GS(th)}\right) \quad (17)$$

Considering the transconductance value from the datasheets, then:

$$t_2 - t_1 = -R_{ON}\left(C_{GD(hv)} + C_{GS}\right) \cdot ln\left(1 - \frac{I_L}{g\left(V_{Dr(on)}-v_{GS(th)}\right)}\right) \quad (18)$$

At instant t_2, the current in the drain stops increasing, and gets equal to I_L. This means that, by (2), from t_2 onwards, the GS voltage is constant and equal to:

$$v_{GSMiller} = v_{GS}(t_2) = v_{GS(th)} + \frac{I_L}{g} \quad (19)$$

This starts the Miller Plateau region that will be discussed later. But first, it must be noted that, for the t_1 to t_2 interval, if the value of the transconductance, g, is taken from the datasheets, and the value of the current, I_L is given in the circuit, then the final value of $v_{GSMiller}$ cannot be freely chosen. This implies that the Miller voltage might be different than the one take from the datasheet, which indeed is a problem for this formulation.

Alternatively, the equation for calculating time t_2 can be obtained using (15) and (16), considering that the value of $v_{GSMiller}$ is taken from the charge plot of the datasheets:

$$t_2 - t_1 = R_{ON} \cdot \left(C_{GD(hv)} + C_{GS}\right) \cdot ln\left(\frac{V_{DR(on)}-v_{GS(th)}}{V_{DR(on)}-v_{GSMiller(datasheet)}}\right) \quad (20)$$

- Interval t_2-t_3: the Miller Plateau.

The key phenomenon in the Miller Plateau is the discharging of C_{GD}. Due to the so-called Miller effect, no current flows through capacitor C_{GS}. From t_2 to t_3, the capacitances C_{GD} and C_{DS} start to discharge through the DS channel, given that the diode R is effectively turned off, and the DS voltage is no more clamped. This means that v_{DS} starts to decreases from V_0 to 0.

Thus, the interval depends on the value of C_{GD}, and as it was mentioned before, this value changes very significantly with the DS voltage. Therefore, another set of parameters are chosen for the calculation of this interval, and additionally to state the Miller Plateau voltage. Instead of using the capacitances and the transconductances, the values of gate charge will be considered. More accurate results are obtained this way [7].

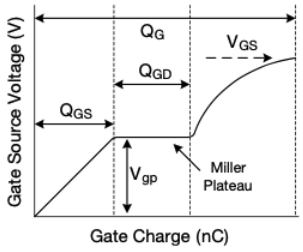

Figure 13 Gate charge as a function of the gate to source voltage, as predicted in [7].

The gate charge plot is summarized in Figure 13. The value of the Miller Plateau will be assumed to be the one represented by this plot, that is usually the one given at the datasheet ratings (and hence, if required, the transconductance, g, would be calculated considering this $v_{GSMiller(datasheet)}$ value):

$$g = \frac{v_{GSMiller(datasheet)}-v_{GS(th)}}{I_L} \quad (21)$$

It must be pointed that the $C_{GD(hv)}$ value is the one that the MOSFET presents at high drain-to-source voltage conditions.

Now, coming back to the Miller Plateau, as commented, the C_{GD} cannot be used a parameter for the equation. It is assumed that during the Miller Plateau, the inductor current is now fully driven by the channel in the drain. Therefore, the current that discharges the C_{GD} capacitor comes solely from the driver. However, thr calculation will be done through charge, not through the equation for the capacitance.

The Miller Plateau can be identified in Figure 13 as the center region, where the slope of the curve is smaller. This corresponds to a charge Q_{GD} that is the difference of the charges in the two knees od the plot (and that is usually presented in the ratings). Tis parameter is going to be assumed as constant (although it changes slightly). It can be said that:

$$I_{Gate} = \frac{dQ_{Gate}}{dt} = \frac{Q_{GD}}{t_3 - t_2} \tag{22}$$

It is also true that:

$$I_{Gate} = \frac{V_{DR(on)} - v_{GSMiller(datasheet)}}{R_{ON}} \tag{23}$$

Therefore, the length of this interval can be assumed to be:

$$t_3 - t_2 = \frac{Q_{GD} \cdot R_{ON}}{V_{DR(on)} - v_{GSMiller(datasheet)}} \tag{24}$$

But the value of Q_{GD} is the value in the datasheet, that might not be consistent to the drain to source voltage value in the actual switching conditions. In order to account for this, it is assumed that the factor Q_{GD}/v_{DS} is kept constant for a given device [7], and therefore:

$$t_3 - t_2 = \frac{Q_{GD(datasheet)}}{v_{DS(datasheet)}} \cdot \frac{v_{DS} \cdot R_{ON}}{V_{DR(on)} - v_{GSMiller(datasheet)}} \tag{25}$$

The Miller Plateau ends in t_3, when v_{DS} reaches zero.

- Interval t_2-t_D

However, the time at which the drain to source voltage remains significant, t_D, is generally speaking smaller than the Plateau interval. This is again because as the reverse capacitance gets discharged, as v_{DS} decreases, its value increases significantly. This means that initially the v_{DS} evolves much faster then at the end of the Miller Plateau. As a consequence, the effective time needs to be calculated. This equation will be considered for the calculation of the power losses at the formula.

In t_D, well before Miller plateau ends, the v_{DS} voltage has already decreased significantly (by an amount of $depth \cdot V_O$). This instant can be calculated considering that the C_{GD} is being discharged through the gate driver:

$$I_{gateON} = \frac{V_{DR(on)} - v_{GSMiller}}{R_{ON}} \tag{26}$$

$$t_{D1} = \frac{C_{GD(hv)} \cdot depth \cdot V_O}{I_{gateON}} \tag{27}$$

$$t_{D2} = \frac{C_{GD} \cdot (1 - depth) \cdot V_O}{I_{gateON}} \tag{28}$$

$$t_D = t_P + t_{D1} + t_{D2} \tag{29}$$

$$t_D - t_P = t_{D1} + t_{D2} \tag{30}$$

- Interval t_3-t_4

At t_3, the gate device finally turns completely on, v_{GS} charges finally from the Miller Plateau to $v_{DR(on)}$, reaching this value finally in t_4.

With the expressions (14)-(25), a formula can be derived for turn on losses:

$$P_{on(i)} = \left[\frac{V_O \cdot I_L}{2}(t_2 - t_1) + \frac{V_O \cdot I_L}{2}(t_3 - t_2)\right] \cdot f_{SW} \tag{31}$$

where intervals t_2-t_1, and t_3-t_2 are given by (20) and (25) respectively.

b) Turn-off Switching Transient with Reverse Recovery Phenomenon in Rectifying Diode.

If the rectifier diode is a real diode with reverse recovery phenomenon, then the waveforms change significantly. This reverse recovery transient implies switching waveforms like the ones in Figure 14.

- Interval t_2-t_P

The evolution of the waveforms until t_2 remains the same than in the previous case, and therefore (20) is valid for calculating t_2-t_1. However, the reverse recovery peak takes place now at time instant t_P.

Knowing the reverse recovery peak current, I_{rr}, and the current slope given by:

$$\frac{di_L}{dt} = \frac{I_L}{t_2 - t_1} = \frac{I_L}{R_{ON} \cdot (C_{GD(hv)} + C_{GS}) \cdot ln\left(\frac{V_{DR(on)} - v_{GS(th)}}{V_{DR(on)} - v_{GSMiller(datasheet)}}\right)} \tag{32}$$

then the value of time t_P can be estimated:

$$t_P - t_2 = \frac{I_{rr}}{\frac{di_L}{dt}} \tag{33}$$

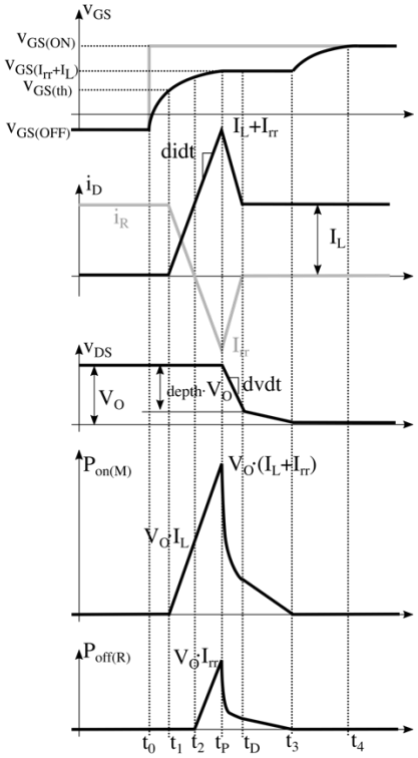

Figure 14 Waveforms at turn on (real rectifier diode).

The value of I_{rr} is not easy to calculate, usually being complex and sensitive to different parameters. In particular, I_{rr} is a function generally of the value of the derivative of the current di_L/dt, of the initial i_L current value, and of the junction temperature. Depending on how this information is given at the datasheets, two situations will be considered for the calculation of I_{rr}.

i. Datasheets without detailed information of Irr

Usually, at the diode datasheet there is no further information than a value of I_{rr} for a given di_L/dt and a given i_L. As a first approach, this value of I_{rr} can be used for the losses calculation:

$$I_{rr} = I_{rr}@datasheet \tag{34}$$

In the case that more precision is required, then the following value will be estimated, applying a rule of thumb:

$$I_{rr}\left(i_L, \frac{di_L}{dt}\right) = I_{rr}@datasheet \cdot \frac{i_L}{i_L@datasheet} \cdot \frac{\frac{di_L}{dt}}{\frac{di_L}{dt}@datasheet} \tag{35}$$

However, this equation needs to be validated either through simulations or (if possible) through experiments.

ii. Datasheets with detailed information of I_{rr}

Otherwise, in the case that the datasheet states a graphical dependency, then the procedure will be as in Annex II.

Therefore, I_{rr} will be defined either by equation (35) or by equation **Error! Reference source not found.**.

In any case, once t_P is calculated, then the value of t_P-t_1 is given, considering (20) and (33):

$$t_P - t_1 = R_{ON} \cdot \left(C_{GD(hv)} + C_{GS}\right) \cdot ln\left(\frac{V_{DR(on)} - v_{GS(th)}}{V_{DR(on)} - v_{GSMiller(datasheet)}}\right) + \frac{I_{rr}}{\frac{di_L}{dt}} \tag{36}$$

- Interval t_P-t_D

Also, again at t_D, well before Miller plateau ends, the v_{DS} voltage has already decreased significantly (by an amount of depth·V_O in Figure 14). This instant can be calculated considering that the C_{GD} capacitor is being discharged through the gate driver, now for the new Miller voltage:

$$I_{gateON} = \frac{V_{DR(on)} - v_{GSMiller(Irr)}}{R_{ON}} \tag{37}$$

$$t_{D1} = \frac{C_{GD(hv)} \cdot depth \cdot V_O}{I_{gateON}} \tag{38}$$

$$t_{D2} = \frac{C_{GD} \cdot (1 - depth) \cdot V_O}{I_{gateON}} \tag{39}$$

$$t_D = t_P + t_{D1} + t_{D2} \tag{40}$$

$$t_D - t_P = t_{D1} + t_{D2} \tag{41}$$

- Interval t_P-t_3

From t_P to t_3, similarly as what happened before, v_{DS} decreases from V_O to 0. This interval can be calculated as in the previous way:

$$t_3 - t_P = \frac{Q_{GD}(datasheet) \cdot}{v_{DS}(datasheet)} \frac{v_{DS} \cdot R_{ON}}{V_{DR(on)} - v_{GSMiller(Irr)}} \tag{42}$$

considering now a different Miller plateau voltage, that takes into account the I_{rr} initial peak current value, that affects all the parameters:

$$v_{GSMiller(Irr)} = v_{GS(th)} + \frac{I_L + I_{rr}}{g}$$

For this to be consistent, the value of the transconductance in this formula is taken for the one that would be calculated considering ideal rectification:

$$g = \frac{v_{GSMiller(datasheet)} - v_{GS(th)}}{I_L} \tag{43}$$

And finally, the power loss expression in the Switch at turn-on with the reverse recovery time is considered, is then given from as:

$$P_{on(r)} = \left[\frac{V_O(I_L + I_{rr})}{2}(t_P - t_1) + \frac{V_O \cdot I_{rr}}{3}(t_D - t_P) + \right.$$
$$\left. + \frac{V_O \cdot I_L}{2}(t_D - t_P)\right] \cdot f_{SW} \tag{44}$$

where intervals t_P-t_1 and t_D-t_P are defined by (36) and (41), respectively.

Expression (44) degenerates in expression (31) if I_{rr}=0 (e.g. Schottky diode).

Besides the losses at the MOSFET, the losses at the diode can also be approximated by:

$$P_{Doff} = \frac{1}{2} \cdot C_R \cdot V_O^2 \cdot f_{SW} + \frac{1}{6} \cdot I_{rr} \cdot V_O \cdot (t_P - t_2) \cdot f_{SW} \tag{45}$$

Notice that these are losses at the diode R, not in the built-in diode of S1. This is consistent with the formula expressed in the chapter about power diodes.

X. Turn-off Switching transient with Inductive Load

At turn on, the following intervals take place (see Figure 15).

Initially, nothing happens. From the gating instant, t_0, until the gate voltage equals the value corresponding to the transconductance times i_L, t_1, nothing happens at the Drain.

The following formulas describe the time intervals in the turn-on transient:

$$v_{GS}(t) = V_{DR(on)} - \left(V_{DR(off)} - V_{DR(on)}\right) \cdot e^{-\frac{t - t_0}{R_{OFF} \cdot \left(C_{GD(lv)} + C_{GS}\right)}} \tag{46}$$

$$t_{1'} - t_{0'} = -R_{OFF} \cdot \left(C_{GD(lv)} + C_{GS}\right) \cdot ln\left(\frac{V_{DR(on)} - v_{GSMiller(datasheet)}}{V_{DR(on)} - V_{DR(off)}}\right) \tag{47}$$

where $C_{GD(lv)}$ is the capacitance at low drain to source voltage conditions.

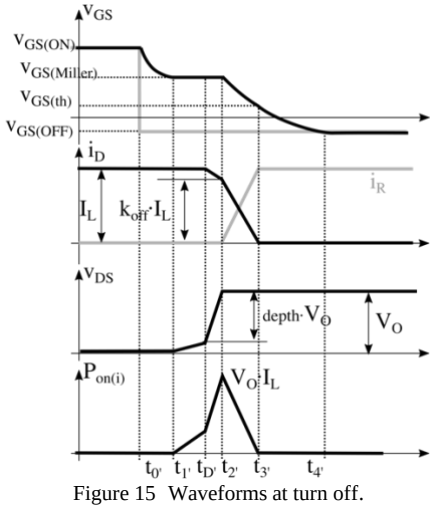

Figure 15 Waveforms at turn off.

$$I_{gateOFF} = \frac{v_{GSMiller(Irr)} - V_{DR(off)}}{R_{OFF}} \quad (48)$$

$$t_{D'1} = \frac{C_{rss} \cdot (1 - depth) \cdot V_O}{I_{gateON}} \quad (49)$$

$$t_{D'2} = \frac{C_{gd(hv)} \cdot depth \cdot V_O}{I_{gateOFF}} \quad (50)$$

$$t_{D'} = t_{2'} - t_{D'1} - t_{D'2} \quad (51)$$

$$t_{2'} - t_{D'} = t_{D'1} + t_{D'2} \quad (52)$$

$$t_{2'} - t_{1'} = \frac{Q_{GD}(datasheet) \cdot}{v_{DS}(datasheet)} \frac{v_{DS} \cdot R_{OFF}}{V_{DR(on)} - v_{GSMiller(datasheet)}} \quad (53)$$

$$t_{3'} - t_{2'} = R_{OFF} \cdot \left(C_{GD(hv)} + C_{GS}\right) \cdot ln\left(\frac{v_{GSMiller(datasheet)} - V_{DR(off)}}{v_{GS(th)} - V_{DR(off)}}\right) \quad (54)$$

And finally,

$$t_{3'} - t_{D'} = t_{3'} - t_{2'} - (t_{2'} - t_{D'}) \quad (55)$$

$$P_{off} = \frac{V_O \cdot I_L \cdot k_{off}}{2} \cdot (t_{3'} - t_{D'}) \cdot f_{SW} \quad (56)$$

Usually, the diode turn-on losses can be neglected. But in any case, only the corresponding contribution of the capacitance in (45) can be used. The parameter k_{off} stands for a decrease in the i_L prior to reaching the end of the Miller Plateau.

XI. Complete Switching Power Losses Expressions in Inductive Switching

Finally, Annex II summarizes the data required and formulas for calculating the power losses in a Power MOSFET and the associated rectifying diode in the inductive switching case.

XII. Resistive Switching Characteristics and Power Losses

Although the inductive switching is by far the most commons type of commutation in power transistors, other conditions might be found in specific converters. The most typical ones are resistive switching, natural switching, and resonant switching.

In this section, resistive switching will be considered. In this situation, the load is assumed to be a resistance, as in Figure 16.

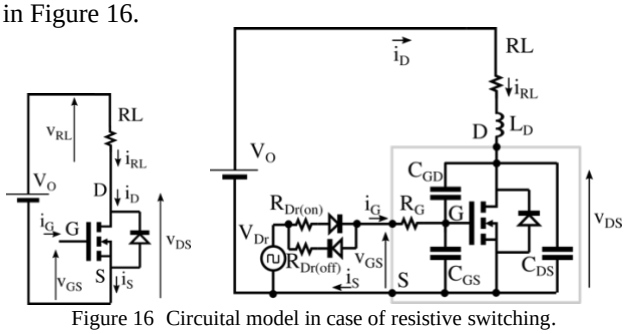

Figure 16 Circuital model in case of resistive switching.

XIII. Turn-on Power Losses in Resistive Switching

The phenomena that take place in the resistive switching are simpler that the ones during inductive switching.

The equations are, in this case, the following:

- Interval t_1-t_0

$$t_1 - t_0 = -R_{ON} \cdot \left(C_{GD(hv)} + C_{GS}\right) \cdot ln\left(1 - \frac{V_{GS(th)} - V_{DR(off)}}{V_{DR(on)} - V_{DR(off)}}\right) \quad (57)$$

- Interval t_3-t_1

$$t_3 - t_1 = \frac{Q_{GD}(datasheet) \cdot}{v_{DS}(datasheet)} \frac{v_{DS} \cdot R_{ON}}{V_{DR(on)} - v_{GS(th)}} \quad (58)$$

- Interval t_2-t_1

$$I_{gateON} = \frac{V_{DR(on)} - v_{GS(th)}}{R_{ON}} \quad (59)$$

$$t_{21} = \frac{C_{GD(hv)} \cdot depth \cdot V_O}{I_{gateON}} \quad (60)$$

$$t_{22} = \frac{C_{GD} \cdot (1 - depth) \cdot V_O}{I_{gateON}} \quad (61)$$

$$t_2 - t_1 = t_{21} + t_{22} \quad (62)$$

Finally, the losses can be estimated by:

$$P_{on} = \frac{V_O \cdot I_L}{6} (t_2 - t_1) \cdot f_{SW} \quad (63)$$

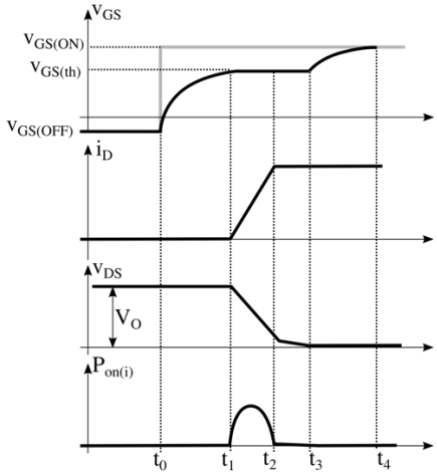

Figure 17 Waveforms at turn on.

XIV. Turn-off Power Losses in Resistive Switching

Similarly, the equations can be described as:

- Interval $t_{1'}$-$t_{0'}$

$$t_{1'} - t_{0'} = -R_{OFF} \cdot \left(C_{GD(lv)} + C_{GS}\right) \cdot ln\left(1 - \frac{V_{DR(on)} - V_{GS(th)}}{V_{DR(on)} - V_{DR(off)}}\right) \quad (64)$$

- Interval t_3-t_1

$$t_{3'} - t_{1'} = \frac{Q_{GD}(datasheet) \cdot}{v_{DS}(datasheet)} \frac{v_{DS} \cdot R_{OFF}}{V_{DR(on)} - v_{GS(th)}} \quad (65)$$

- Interval $t_{3'}$-$t_{2'}$

$$I_{gateOFF} = \frac{v_{GS(th)} - V_{DR(off)}}{R_{OFF}} \quad (66)$$

$$t_{21'} = \frac{C_{GD(hv)} \cdot depth \cdot V_O}{I_{gateOFF}} \quad (67)$$

$$t_{22'} = \frac{C_{GD} \cdot (1 - depth) \cdot V_O}{I_{gateOFF}} \quad (68)$$

$$t_{3'} - t_{2'} = t_{21'} + t_{22'} \quad (69)$$

Finally, the losses can be estimated by:

$$P_{off} = \frac{V_O \cdot I_L}{6} (t_{3'} - t_{2'}) \cdot f_{SW} \quad (70)$$

Besides the losses at the MOSFET, the losses at the diode can also be approximated by:

$$P_{Doff} = \frac{1}{2} \cdot C_R \cdot V_O^2 \cdot f_{SW} \quad (71)$$

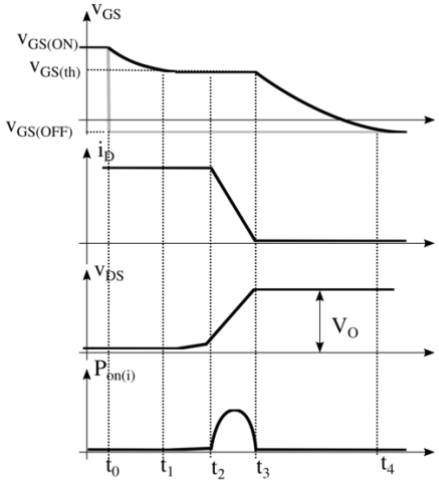

Figure 18 Waveforms at turn off.

XV. Switching Characteristics in Resonant Converters and Power Losses

Figure 19 represent a series resonant converter. Figure 20 shows the waveforms for resonant inductive switching, while Figure 21 shows the same diagram for resistive capacitive waveforms.

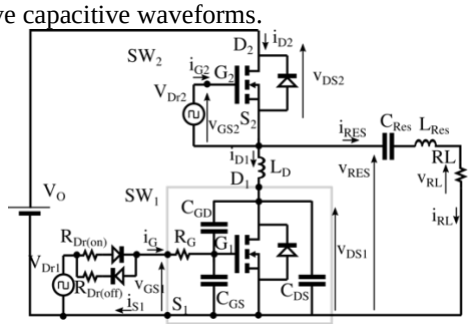

Figure 19 Diagram of RLC series resonant circuit

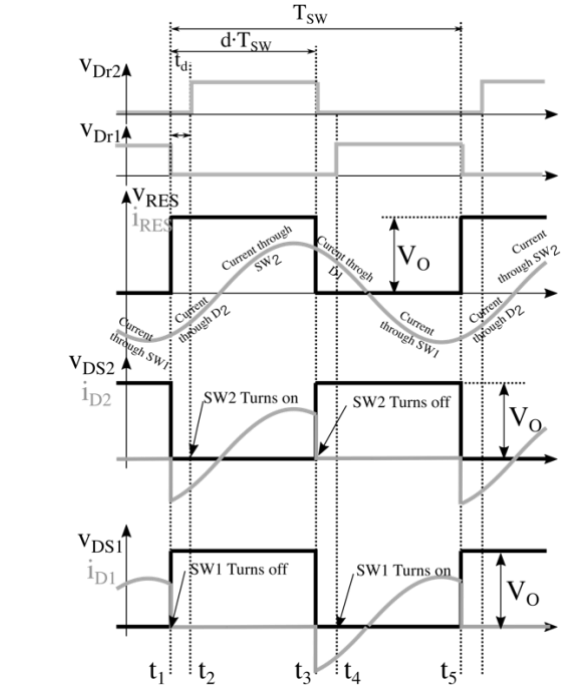

Figure 20 Waveforms in resonant circuit, for inductive behavior.

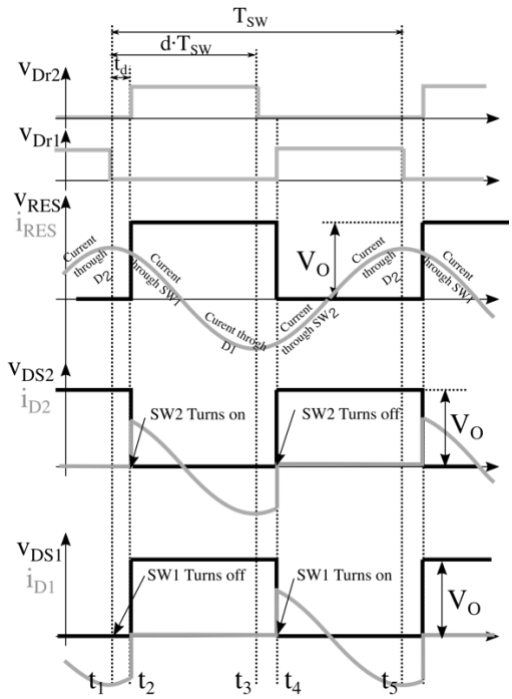

Figure 21 Waveforms in resonant circuit, for capacitive behavior

It can be summarized that the follow applies when talking about resonant switching:

- For resonant inductive switching (switching at a frequency higher than the resonant in a LC-SRC or LLC-SPRC): No turn on losses, while turn off losses have same formulas than inductive switching.
- For resonant capacitive switching (switching at a frequency lower than the resonant in a LC-SRC or LLC-SPRC): Turn on losses have same formula than inductive hard switching (with reverse recovery effect), while turn off losses can be neglected.
- For resonant resistive switching (just at resonant frequency), there are no switching losses.

XVI. Conclusions

The steady state operation and switching transients on a Power MOSFET have been studied. Finally, the detailed expressions for the power losses calculation of the transistors are obtained.

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