Power Diodes Basics

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I. Introduction

The following is a basic introduction to obtaining the static characteristics of power semiconductors. Then, the main operating states in power applications will be identified. After that, the dynamic characteristics (switching waveforms) will be discussed.

Ultimately, the switching and conduction losses in semiconductors will be analyzed.

Finally, a summary of soft-switching techniques will be discussed, including ZVS-ZCS techniques, resonant converters and snubbers.

II. Static Characteristic of Power Diodes

a) Intrinsic semiconductor

A conductor is a lattice in which charge carriers, namely electrons, (-), are free and might move by thermal excitation, although globally the lattice is neutral. The global direction of movement depends on mainly two conditions:

- On the concentration gradient, where carriers move towards decreasing concentrations of carriers,
- On an external electric field, where the carriers move accordingly the sign of the field.

In any case, internally, the field within the conductor is null.

The total current can be defined as:

$$i = \frac{Q^-}{\tau_T} \quad (1)$$

Where Q^- is the total mobile electron charge, and τ_T is the transit time [1].

On the other hand, semiconductors can be understood basically as insulators. The following picture schematizes a semiconductor lattice, of intrinsic (I) material, e.g. Silicon, Si. At 0 K, all the electrons in the atoms are bonded to the nuclei, and thus there are not unbonded ion-electron pairs able to carry charge.

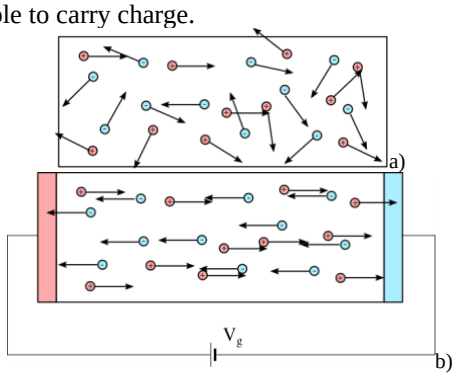

Figure 1 Intrinsic silicon scheme. a) Random movement due temperature (any instant concentration mismatch is compensated through diffusion processes). b) Movement due an external field.

At room temperature, the thermal energy in the lattice creates a small number of unbonded ion-electron pairs. This implies the existence of negative carriers, in this case electrons (-) and positive carriers, holes (+). These charge carriers might move randomly. But in any case, the lattice presents a global zero electrical charge, as sworn in Fig 1.a.

This movement is aligned provided that the external voltage conditions are adequate (Figure 1.b).

However, this current flow is not easy, and therefore the equivalent resistance of the intrinsic silicon material is high (it is an insulating material).

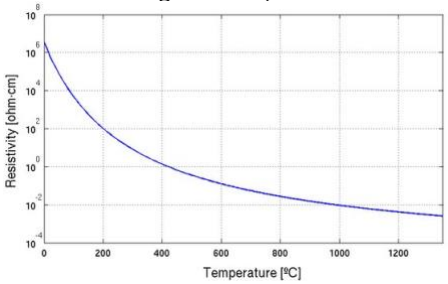

Figure 2 Variation of silicon resistivity vs. temperature [2]

b) PN-Junction.

Silicon can be doped by materials of group V, for instance Phosphorus. These materials easily diffuse in the lattice when forming the substrate, and release an electron, (-), forming a positive Ion [+]. These dopants are called donors. This results in a N region, where a lot of (-) appear, most of them provided by the donors. These are the majority carriers. However, a minority of holes (+), formed by thermal, are also present., and a minority of holes.

Analogously, group III materials create a P region, with a majority of (+), provided by the ions of the acceptor, [-], and a minority of (-) produced by thermal causes.

In any case, the lattice is electrically neutral. Figure 3 shows a P and a N region, with a representation of the majority and minority carriers in each region. The interface is separated, no interaction between the 2 regions is present.

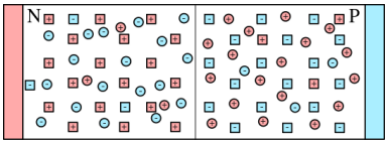

Figure 3 N and P regions.

When both regions are interfaced, the physical system is called PN junction. In a PN junction, the N region is called cathode, and the P region is called anode there is a transient diffusion of majority (-) towards the P region, due the concentration gradient. Same thing happens with majority (+), diffusing toward the N region. Pairs (+)(-) recombine, resulting in a net charge barrier appearing in the interfacing surface.

This net charge implies an electric field that opposes the flow of the majority chargers. Take the (-) at the left of figure 4.a, where they are majority carriers in the N region.

These (-) tend to diffuse towards the P region, following the gradient of concentrations. However, an electric field pointing to the right appears in the depletion region (as the electric field is the force experimented per unit of positive charge). Therefore, the (-) tend to move back towards the N region as a result of this field. Therefore, further recombinations are prevented by this field.

The depletion region has a given length, where no carriers are present. In addition, any charger there is accelerated by the existing field. Notice that minority carriers flow due this electric field at the depletion region, but in this case the concentration tends to avoid the flow.

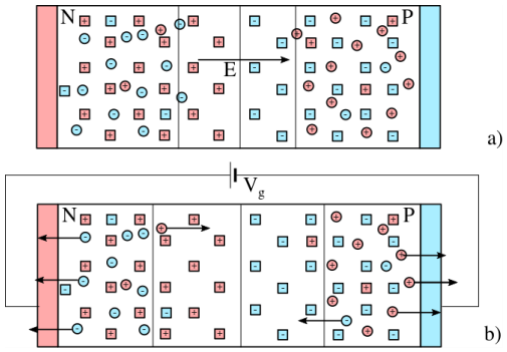

Figure 4 a) NP junction. b) Reverse bias.

c) Reverse and Forward bias

When an external field is connected with the polarity in Figure 4.b, reverse bias conditions are met. Charges tend to move accordingly. In N region, (+) are injected and (-) are removed. Given that the lattice far from the depletion region has moving charges, therefore it behaves as a conductor, and the field is null there. The charge carriers move due the gradient of concentrations. The majority carriers tend to move apart from the depletion region, whereas the minority carriers flow toward this region. This results on an increase of the depletion region width.

The same phenomenon happens in the P region. The external filed is added to the depletion field, and is concentrated in the depletion region.

This results globally on no current flowing, and the device withstanding the external field (and therefore the external voltage).

On the other hand, if the external field opposes the depletion field, resulting in a forward bias (Figure 4.c), then the situation is different. In the N region, (-) are injected, and these carriers have enough energy as to reach the P region, where they are minority carriers. These minority carriers will eventually recombine with (+), resulting in a net current flow. Same thing applies to (+) in the P region.

Therefore, the junction current is related directly to the charge flow due the minority carriers in both sides of the depletion region.

In steady state, this is true for every cross-sectional surface in the junction.

Some initial field is required to surpass the depletion field.

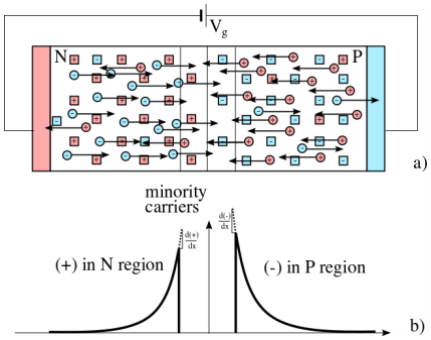

Figure 5 a) Forward bias. b) Distribution of minority carriers in steady state.

d) Static characteristic

Figure 6 shows the typical PN junction electric symbol, i.e. a diode, together with the usual references for voltage and current in the diode. The characteristic shows the main regions of operation, the forward bias region (positive current) and the reverse bias region (negative voltage region). The relationship between the voltage and current is given by the Shockley equation:

$$i = I_S\left(e^{\frac{v}{n \cdot V_T}} - 1\right) \tag{2}$$

being

$$V_T = \frac{k \cdot T}{q} \tag{3}$$

$$I_S = \frac{Q_0}{\tau_L} \tag{4}$$

where I_S is the reverse bias saturation current, V_T is the thermal voltage, k is the Boltzmann constant, q is the electron charge, Q_0 is a constant that depends on the dopant concentrations, τ_L is the minority carrier lifetime, and n is an ideality factor, depending on the material.

During forward operation, the voltage through the diode must be higher than an initial value, the forward voltage, u_F, in order to allow the current flow. Therefore, the most simple model considers a voltage source accounting for this drop, together with a small dynamic resistor, r_d, that accounts for the slope when current increases.

On the reverse operation, there is a maximum reverse voltage that the diode is able to withstand, u_{RM}. IN addition, a very small reverse current flows, but it can generally be neglected.

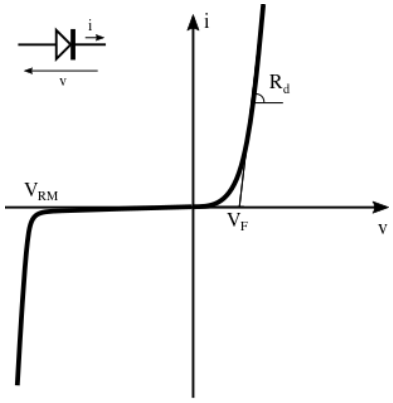

Figure 6 Static Characteristic of a diode.

e) Equivalent circuit

The equivalent circuit for both regions is depicted in figure 6. Notice that both the u_F and the r_d depend on parameters such as the operating current, temperature, etc.

f) Operation limits

In steady state, the forward operational limits come from the maximum average current the device can carry, at a given temperature. This limit is established based on the power dissipation due the forward voltage.

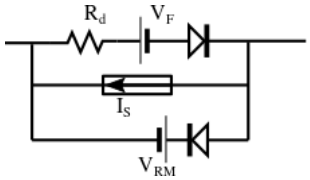

Figure 7 Static Characteristic of a real diode.

The reverse operation is limited to the reverse voltage (continuous, pulsed, etc.).

III. Conclusions

The static performance of a diode depends on the concentration of charge carriers within the doped region so the semiconductor lattice. This behavior is studied and the main performance characteristics is discussed in this report.

REFERENCES

[1] Fundamentals of Power Electronics, Ed. 2001, Robert W. Erickson, Dragan Maksimović, Springer US, ISBN 9780306480485

[2] “Understanding and improving the chemical vapor deposition process for solar grade silicon production”, Alba Ramos, February 2016, DOI: 10.13140/RG.2.1.3387.1122,