Cascaded Loop Control of a DC to DC Boost Converter

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***Abstract* – This report shows a step-by-step guide of how to control a given power topology (boost converter) controlling both the inductor current ant the capacitor voltage by means of separate control loops.**

Although the methodology is explained for the output voltage control in a given boost converter, the procedure can be implemented to control other parameters (e.g. input voltage control) or even to control parameters in other DC-to-Dc converters, such as Buck, Buck-Boost or Cûk converters.

***Keywords* – DC to DC converters control, nested control loops, Regulator calculation.**

I. Introduction

The following discussion is intended to provide a step-by-step procedure to design the controllers in a nested loop control scheme. In this example, the idea is to control the output voltage of a Boost converter, where the load is formed by a parallel connection of a capacitor C and a resistor R. However, the procedure can be implemented to control other output circuits (e.g. considering Equivalent Series Resistor of the capacitor, or additional resistive parasitic components), different variables (e.g. input voltage control) or even to control parameters in other DC-to-DC converters, such as Buck, Buck-Boost or Cûk converters.

All the discussion of this report is related to the power scheme of fig. 1, with the following considerations:

•The transistor and the diode are supposed to be ideal components

•The parameter to be controlled is the output voltage, U_O.

•The system operates at continuous conduction mode (CCM) at steady state.

•All the voltage and currents present small switching frequency ripple.

•The inductor has a series resistor accounting for the copper losses.

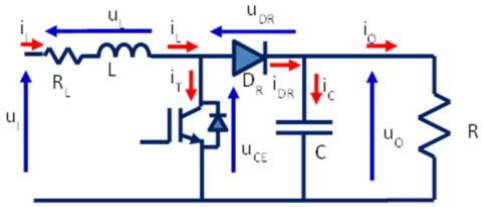

Fig. 1. Power stage of a boost converter, with voltage and current references.

There are two approaches to control the output voltage (capacitor voltage) in this power converter. The first option is to consider the full transfer function between the variable to be controlled, U_O, and the control signal, the duty ratio of the transistor, d.

In this case, the control system can be represented as in fig. 2.

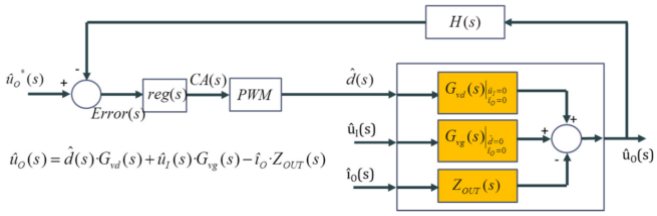

Fig. 2. Control System Block Diagram with single regulator.

The small-signal model of the system provides a transfer function that has the following expression:

$$\frac{\hat{v}_0(s)}{\hat{d}(s)} = \frac{V_0}{(1-D)} \cdot \frac{1-\frac{L}{(1-D)^2 \cdot R}\cdot s}{1+\frac{L}{(1-D)^2 \cdot R}\cdot s+\frac{L\cdot C}{(1-D)^2}\cdot s^2} \qquad (1)$$

Equation (1) can be re-written to be expressed in a canonical form:

$$\frac{\hat{v}_0(s)}{\hat{d}(s)} = G_{d0} \cdot \frac{1-\frac{s}{\omega_z}\cdot s}{1+\frac{s}{Q\cdot\omega_0}+\frac{s^2}{\omega_0^2}} \qquad (2)$$

This equation represents a second order system with a right half-plane (RHP) zero, what yields to some problems when controlled by a single regulator.

The other control approach, intended to solve this last issue, is to control the output voltage by means of two nested control loops, each one of them controlling a first-order system, as it is depicted in figure 3.

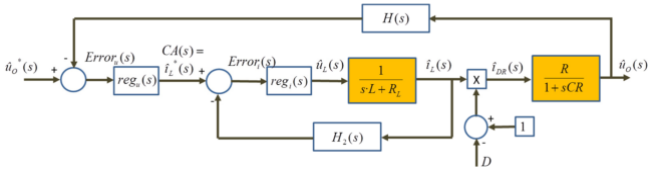

Fig. 3. Control System Block Diagram with two nested control loops

This decouples the control of the inductor current from the control of the capacitor voltage, yielding to a much more versatile control strategy.

However, the main drawback of this system is that the current of the inductor must be measured, in addition to the input and output voltage values must be measured.

II. The Output Voltage Control Loop

The key idea of controlling the output voltage control loop is to consider that the input control loop is much faster

than the outer one. Hence, this methodology implies that the dynamics of the control loops are clearly decoupled.

Thus, from the point of view of the outer voltage loop, the current control is instantaneous (*much faster*). If so, then the outer voltage loop can be considered as the one in fig. 4.

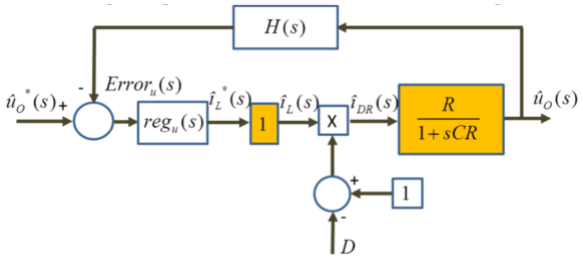

Fig. 4. Output voltage control loop

The identity block, '1', accounts for the inner current control circuit, and will be discussed in the following section.

Considering that the sensor has no dynamics, H(s)=1, the final transfer function, from $\hat{\imath}_L(s)$ to $\hat{u}_O(s)$, can be calculated as:

$$\frac{\hat{v}_0(s)}{\hat{\imath}_L(s)} = \frac{\hat{v}_0(s)}{\hat{\imath}_{DR}(s)} \cdot \frac{\hat{\imath}_{DR}(s)}{\hat{\imath}_L(s)} = \frac{R}{1+s\cdot C\cdot R} \cdot \frac{1}{1-D} \qquad (3)$$

Obviously, it is a first order system. The considered regulator is a PI controller, and it will be tuned by means of pole cancellation.

The expression of the PI can be expressed as:

$$REG_u(s) = K_{PV} \cdot \left(1 + \frac{1}{s\cdot T_{IV}}\right) = K_{PV} \cdot \frac{1+s\cdot T_{IV}}{s\cdot T_{IV}} \qquad (4)$$

The condition imposed by the pole cancellation is:

$$T_{IV} = R\cdot C \qquad (5)$$

Upon that condition, the final transfer function of the full system, is:

$$G'(s) = \frac{REG_v(s)\cdot G(s)}{1+REG_v(s)\cdot G(s)} = \cdots = \frac{1}{1+s\cdot\frac{T_{IV}}{\frac{K_{PV}}{1-D}\cdot R}} \qquad (6)$$

And the value of K_{PV} that provides a final dynamic response of a given bandwidth, BW_V, is:

$$K_{PV} = 2\cdot\pi\cdot BW_V\cdot C\cdot(1-D) \qquad (7)$$

It must be noticed how the exact characteristics of the behavior of the regulator are calculated for a single operation point.

III. The Inner Current Loop

The inner control loop is depicted in figure 5, as discussed previously. Again, it will be considered that the sensor has no dynamics, H(s)=1.

The regulator is another PI controller, with a similar expression:

$$REG_I(s) = K_{PI} \cdot \frac{1+s\cdot T_{II}}{s\cdot T_{II}} \qquad (8)$$

a) Tuning the inner loop through pole-cancellation method.

Using the pole cancellation approach, then the following condition appears:

$$T_{II} = \frac{L}{R} \qquad (9)$$

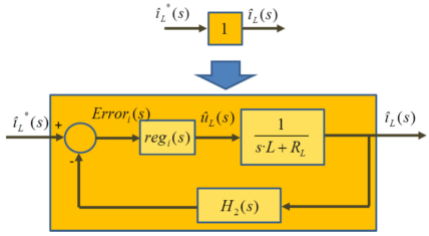

Fig. 5. Inner current control loop

The closed loop transfer function is now:

$$G_I'(s) = \frac{REG_i(s)\cdot G(s)}{1+REG_i(s)\cdot G(s)} = \cdots = \frac{1}{1+s\cdot\frac{T_{II}}{K_{PV}\cdot R_L}} \qquad (10)$$

The value of K_{PI} that provides a final dynamic response of a given bandwidth, BW_i, is then:

$$K_{PI} = 2\cdot\pi\cdot BW_i\cdot L \qquad (11)$$

However, the pole-cancellation scheme followed for the voltage control might not be very effective, since the value of the parasitic series resistor of the filter, R_L, is by definition small, and might change significantly with operating parameters such as temperature or current levels.

b) Tuning the inner loop with the general procedure

Instead, the filter can be assumed as a pure integrator for the PI tuning. A simple proportional controller is not acceptable, though, since the small resistor present in the real device would provide errors.

For a PI defined analogously as in the voltage loop case:

$$PI_i(s) = K_{PI} \cdot \left(1 + \frac{K_{II}}{s}\right) \qquad (11)$$

Then the closed loop response, considering a pure inductor L, is given by:

$$G_{CLi} = \frac{1+\frac{1}{K_{II}}\cdot s}{1+\frac{1}{K_{II}}\cdot s+\frac{L}{K_{II}\cdot K_{PI}}\cdot s^2} \qquad (12)$$

Identifying terms with the second order expression as a function of the natural frequency, f_n, and the damping factor, ζ,

$$G_{CLi} = \frac{1+\frac{1}{K_{II}}\cdot s}{1+\frac{1}{K_{II}}\cdot s+\frac{L}{K_{II}\cdot K_{PI}}\cdot s^2} = \frac{1+\frac{2\cdot\zeta}{2\cdot\pi\cdot f_n}\cdot s}{1+\frac{2\cdot\zeta}{2\cdot\pi\cdot f_n}\cdot s+\left(\frac{1}{2\cdot\pi\cdot f_n}\right)^2\cdot s^2} \qquad (13)$$

then the following relations that define the PI controller can be derived,

$$K_{PI} = 4\cdot\pi\cdot BW_i\cdot L\cdot\zeta \qquad (14)$$

$$K_{II} = \frac{2\cdot\pi\cdot BW_i}{\zeta} \qquad (15)$$

where it has been considered that the bandwidth of the current control loop, BW_i, is equal to the natural frequency, f_n.

IV. Implementation of the Cascaded Control

Both control loops have been designed for a given operation point. However, the duty ratio needed to drive the power switch of figure 1 has not been calculated on the previous discussion.

In fact, the inner loop must provide this duty ratio to be implemented by the power drivers.

The basic idea is that the $\hat{\imath}_L(s)$ to $\hat{v}(s)$ block, i.e. the plant of the inner loop, is a virtual plant; the actual plant is a power converter, or more accurately, the transfer function between the duty ratio, $\hat{d}(s)$, and the inductor current, $\hat{\imath}_L(s)$:

$$G_{iLd}(s) = \frac{\hat{\imath}_L(s)}{\hat{d}(s)} \qquad (16)$$

Thus, it is necessary to adapt the information coming from the control action, $\hat{v}_L(s)$, to the duty ratio, $\hat{d}(s)$, by means of the scheme depicted in figure 6, yielding to the following final expression:

$$G_i(s) = \frac{\hat{\imath}_L(s)}{\hat{v}(s)} = \frac{\hat{d}(s)}{\hat{v}_L(s)} \cdot \frac{\hat{\imath}_L(s)}{\hat{d}(s)} = \frac{\hat{d}(s)}{\hat{v}_L(s)} \cdot G_{iLd}(s) \qquad (17)$$

Finally, the expression needed to calculate the value of d(s) from the value of the inductor voltage, $\hat{u}_L(s)$, is:

$$\hat{d}(s) = \frac{\hat{v}_L(s) - \hat{v}_i(s)}{\hat{v}_o(s)} - 1 \qquad (18)$$

This last expression is calculated from the steady state conditions on the converter.

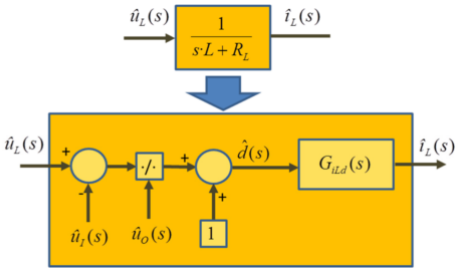

Fig. 5. Implementation of control loops – calculation of duty ratio

IV. Conclusions

A step-by-step procedure has been explained for designing the PI controllers in a nested control loops approach. The final goal is to control the voltage at the output of the converter.

The procedure is valid for controlling other kind of loads or of parameters, and even for other kind of converters, and with other type of controllers.

Although only the pole cancellation and the conventional tuning methods have been considered in this report, any other method can be used for tuning the controllers.